DEMO MANUAL DC1840B

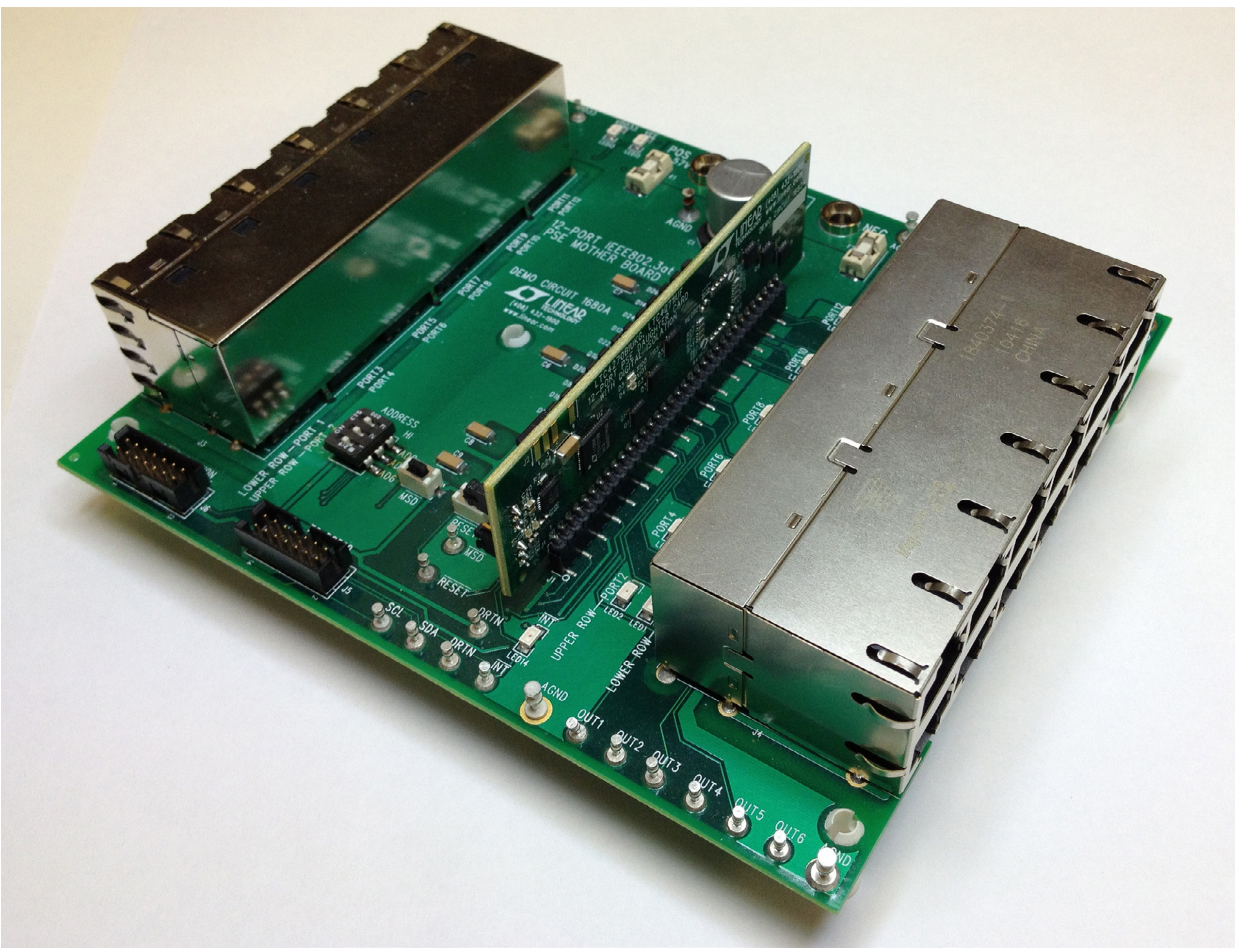
DC1682B and DC1680A LTC4270/LTC4271 12-Port PSE with Digital Isolation

DESCRIPTION

Demonstration kit DC1840B is a 12-port Type 2 power sourcing equipment (PSE) composed of a DC1682B daughter card and DC1680A mother board. The kit is used for evaluation of the LTC4270B and LTC4271 PSE chipset. Up to 12 powered devices (PDs) can be connected and powered from this system using a single power supply. A DC590B is connected to the DC1840B for I^2C interfacing with QuikEval™. This demonstration manual provides a Quick Start Procedure, a DC1682 overview, a DC1680 overview, schematics, and layout printouts. Other available supporting documents for the DC1840 are the LTC4270/LTC4271 Layout Guide and the LTC4271 PSE Demo Software Users Manual.

Design files for this circuit board are available at http://www.linear.com/demo

BOARD PHOTO



QUICK START PROCEDURE

Demonstration kit DC1840B includes the DC1682 daughter card and DC1680 mother board. The kit is set up for evaluating the LTC4270/LTC4271. Follow the procedure below and refer to Figures 1 through 4 for proper equipment setup.

1. On the DC1682 set AUTO jumper JP1 to HI (Figure 1) to enable AUTO pin mode.
2. On the DC1682 set MID jumper JP2 to LO (Figure 1) to disable midspan mode.
3. Align pin 1 of the 34-pin male connector on the DC1682 with pin 1 of the 34-pin female connector on the DC1680 (Figure 2). Pin 12 is polarized to assist with the alignment. Carefully push the DC1682 straight down until the two 34-pin connectors are flush with each other.
4. On the DC1680, connect a supply with the positive rail to POS and negative rail to NEG (Figure 3). Use a power supply capable of sourcing the maximum load expected (12 ports × 850mA ≥ 10.2A). Ramp the supply up to 55V.
5. Connect up to 12 PDs to the DC1680, J4 (Figure 3).
6. The DC590 is optionally connected to the DC1680 connector J5 with a 14-pin ribbon cable (Figure 3). A GUI for the LTC4270/LTC4271 is brought up by QuikEval for I^2C interfacing from a PC (Figure 4).

QUICK START PROCEDURE

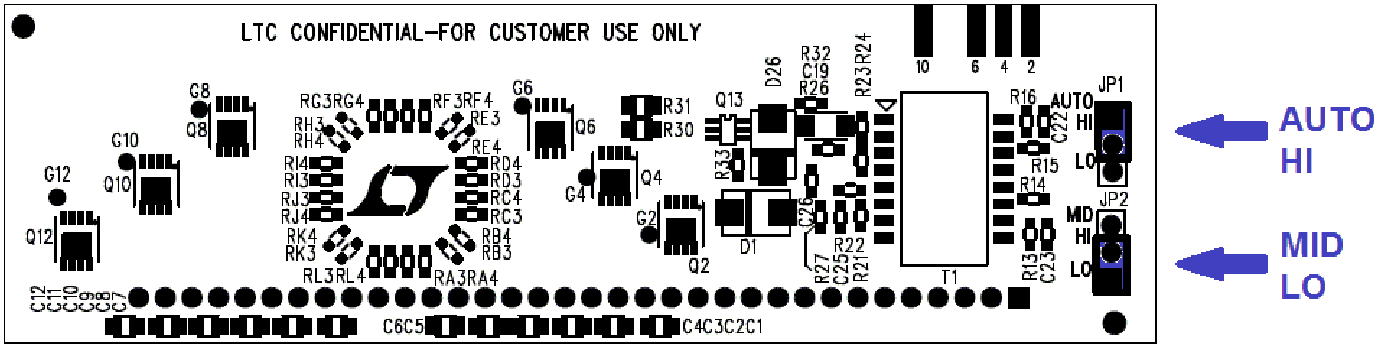


Figure 1. DC1682 Backside. Setting AUTO and MID Jumpers

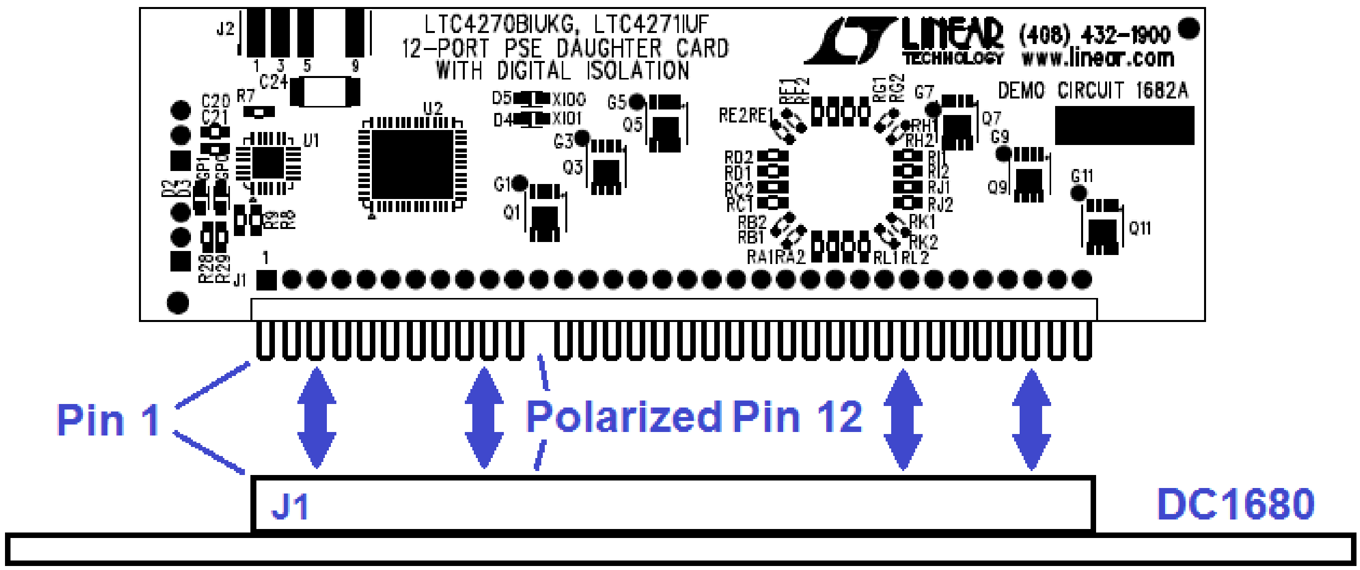


Figure 2. Inserting the DC1682 into J1 of the DC1680

QUICK START PROCEDURE

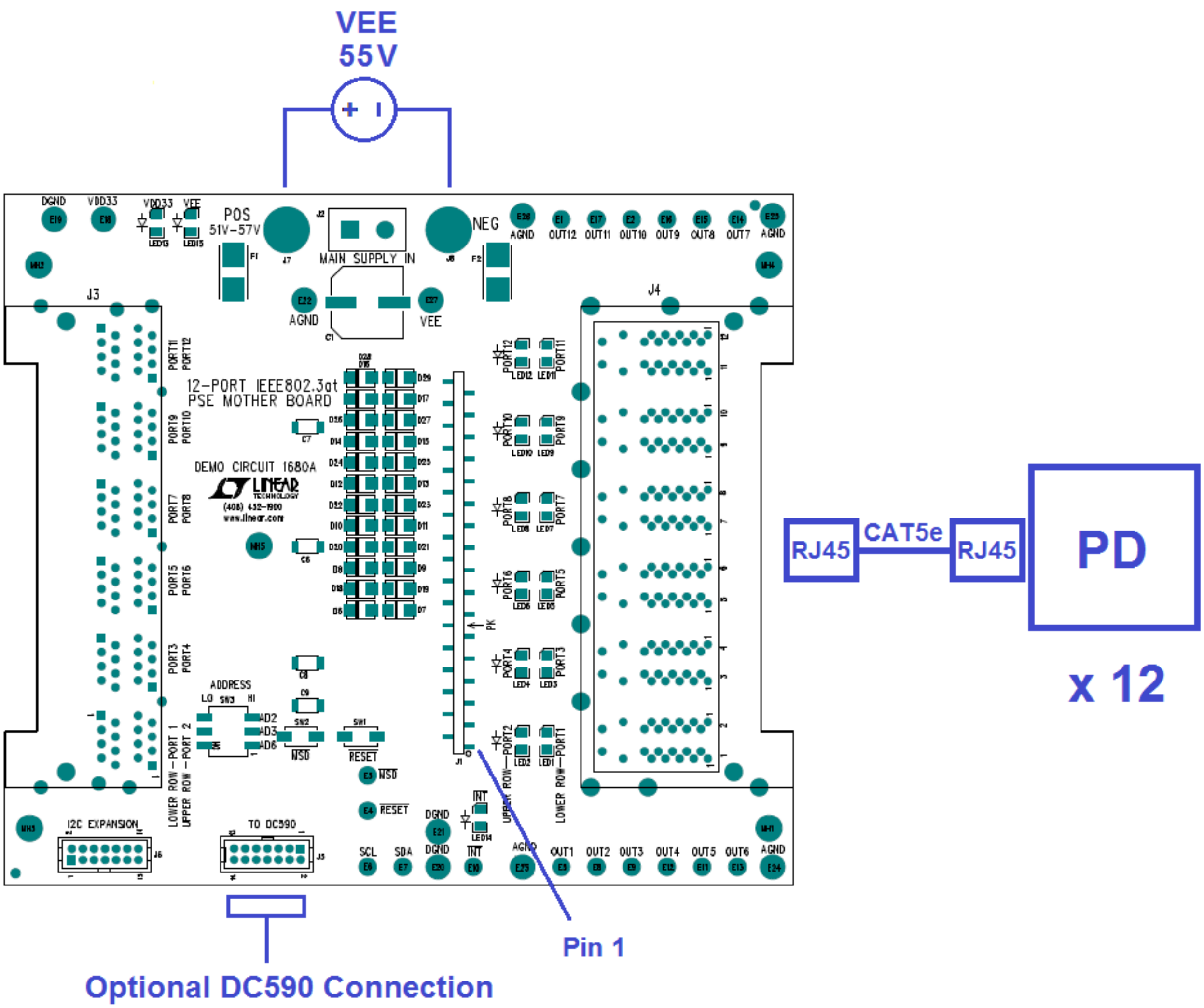


Figure 3. DC1840 Basic Setup

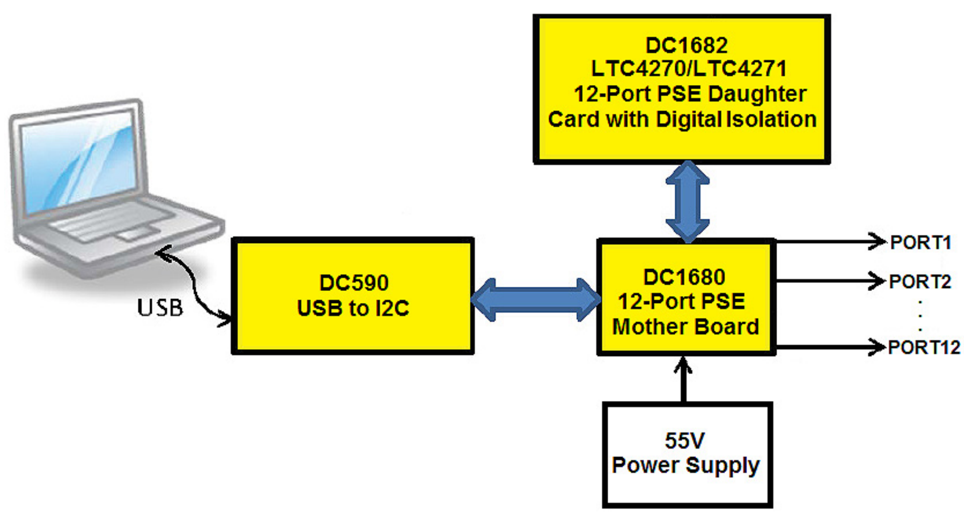


Figure 4. System Setup with the DC590, DC1680, DC1682 and 55V Power Supply

DEMONSTRATION CIRCUIT 1682B OPERATION

12-Port PSE Daughter Card with Digital Isolation

Demonstration circuit 1682B (Figure 5) features the LTC4270/LTC4271 chipset on a compact daughter card with digital isolation. The LTC4270/LTC4271 chipset is a 12-port power sourcing equipment (PSE) controller designed for use in IEEE 802.3at Type 1 and Type 2 (high power) compliant Power over Ethernet (PoE) systems. A transformer isolated communication protocol replaces expensive opto-couplers and complex isolated 3.3V supply resulting in significant BOM cost savings. The LTC4270/LTC4271 chipset delivers lowest-in-industry heat dissipation by utilizing low R_{ON} external MOSFETs and 0.25Ω sense resistors, eliminating the need for expensive heat sinks.

Advanced power management features in the LTC4270/LTC4271 chipset include: per port 12-bit current monitoring ADCs, DAC programmable current limit, and versatile quick shutdown of preselected ports. PD discovery uses a proprietary dual mode 4-point detection mechanism ensuring excellent immunity from false PD detection. Midspan PSEs are supported with 2-event classification and a two second backoff timer. The LTC4270/LTC4271 includes an I^2C serial interface operable up to 1MHz.

The DC1682B demonstrates proper LTC4270/LTC4271 board layout that is approximately the height and width of a 2 × 6 RJ45 connector. The compact layout is made possible by the small package size of key components. The LTC4270 is in a 7mm × 8mm QFN, while the LTC4271 is in a 4mm × 4mm QFN. Each port has a FDMC3612 MOSFET in a 3mm × 3mm power33 package.

The daughter card inserts in the DC1680B mother board through J1, a polarized 34-pin connector. Isolated 3.3V and logic control signals are brought in on this connector. Also connected at J1 is the PoE V_{EE} supply from the mother board and 12 PSE controlled outputs.

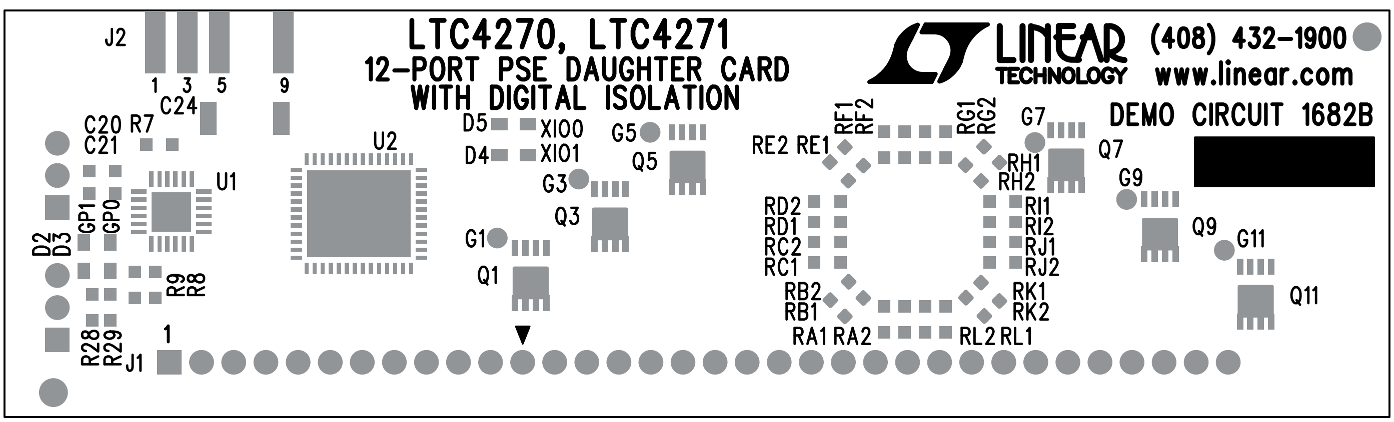


Figure 5. DC1682A 12-Port PSE Daughter Card with Digital Isolation Features the LTC4270 and LTC4271

DEMONSTRATION CIRCUIT 1682B OPERATION

Board Layout

Proper board layout is crucial for proper LTC4270/LTC4271 chipset operation, robustness, and accuracy. When laying out, pay attention to parts placement, Kelvin sensing, power paths, and copper fill. It is imperative to follow the LTC4270/LTC4271 Layout Guide document when laying out the board.

Isolation and Power Supplies

The LTC4270/LTC4271 chipset provides communication across an isolation barrier through a data transformer (Figure 6). This eliminates the need for expensive optocouplers. All digital pins reside on the digital ground reference and are isolated from the analog PoE supply. A 3.3V supply for V_{DD} and an isolated V_{EE} supply are connected to the DC1682B through the 34-pin connector.

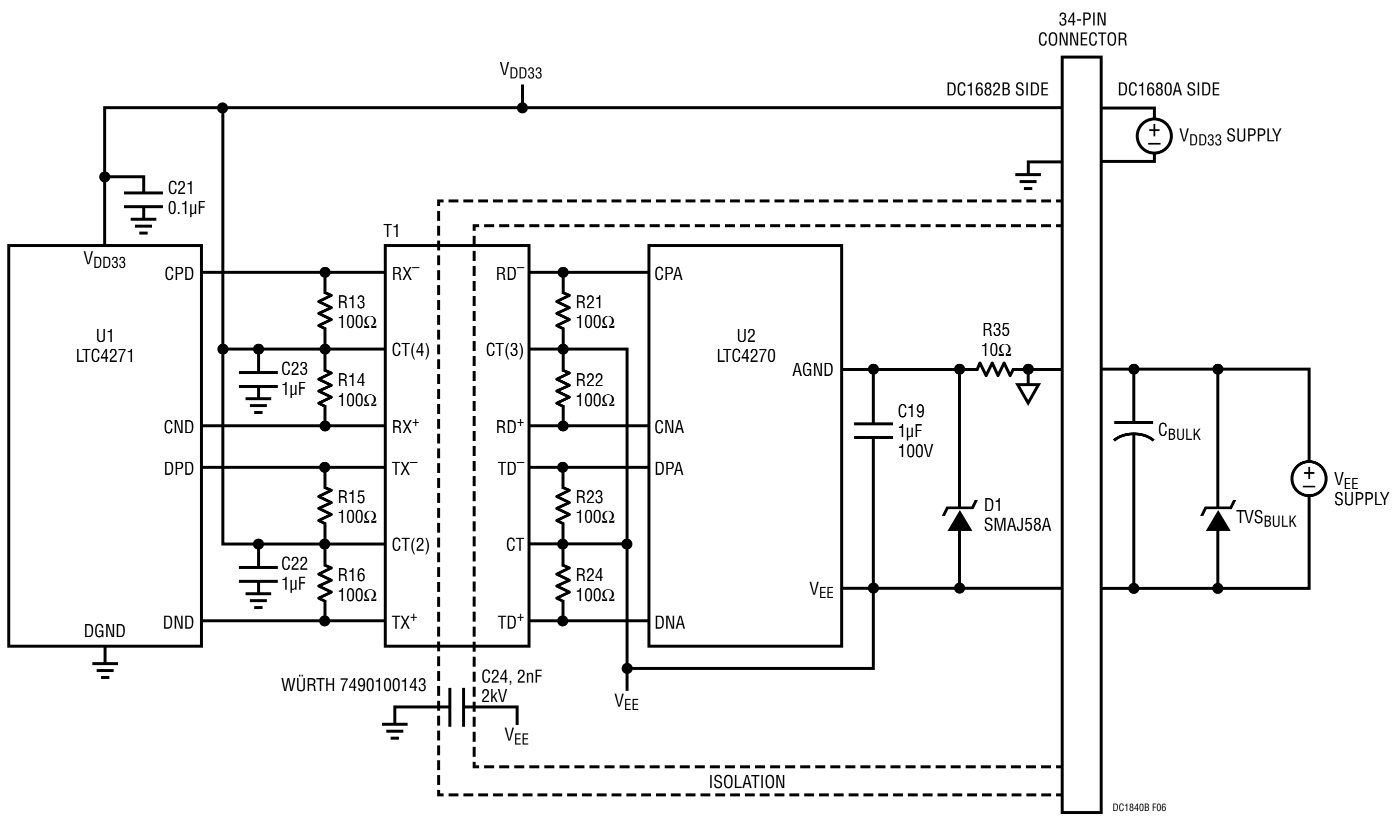


Figure 6. DC1682B Digital and Analog Isolation

DEMONSTRATION CIRCUIT 1682B OPERATION

I²C Communication and Addressing

The LTC4271 internal registers are accessed via I²C to read and/or write configuration, status, and interrupt registers. The I²C lines SDAOUT, SDAIN and SCL connect to the 34-pin connector (Figure 7). Subsequently, the I²C bus is accessed on the DC1680.

The LTC4270/LTC4271 chipset has an address of ($A_6 10 A_3 A_2 A_1 A_0$b), where A_6, A_3, A_2, A_1, and A_0 are the logic state of the AD6, AD3, AD2, AD1, and AD0 pins respectively. On the DC1682B, AD0 and AD1 are tied low with pull-down resistors. AD2, AD3 and AD6 are brought out to the 34-pin connector (Figure 7) and set with three switches on the DC1680.

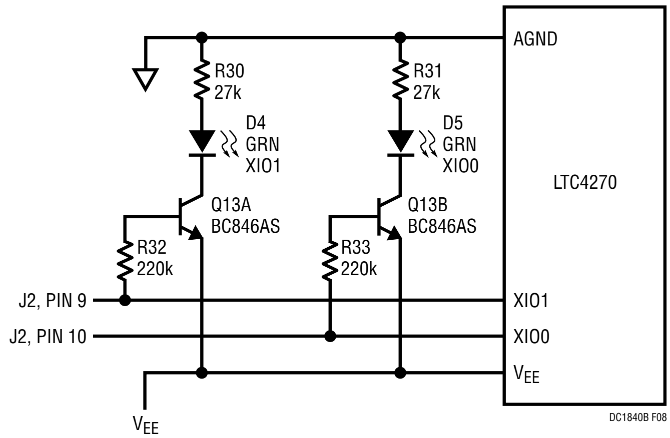


Figure 8. DC1682B, LTC4270 General Purpose I/O LED Indicators

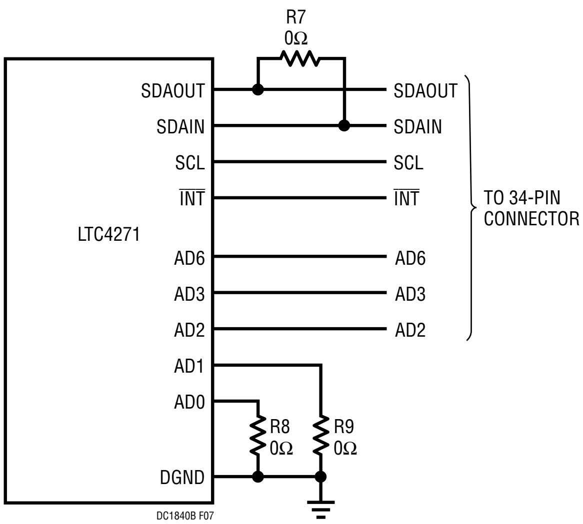


Figure 7. DC1682B LTC4271 I²C and Address Connections

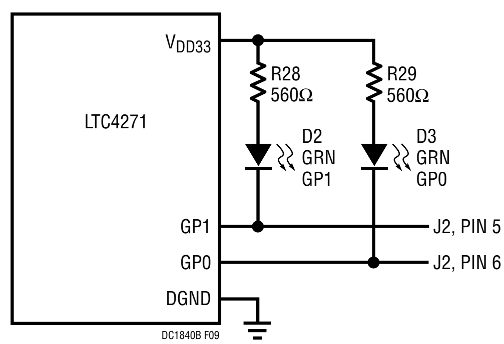


Figure 9. DC1682B, LTC4271 General Purpose I/O LED Indicators

I/O LED Indicators

The DC1682B features four LEDs to indicate the states of the LTC4270/LTC4271 chipset general purpose input output pins. These pins are configured as inputs or outputs via I²C. GP1 and GP0 are referenced to DGND and driven by the LTC4271 when set as outputs (Figure 8). XIO0 and XIO1 are referenced to V_{EE} and are driven by the LTC4270 when set as outputs (Figure 9). J2 provides test points for access to these I/Os.

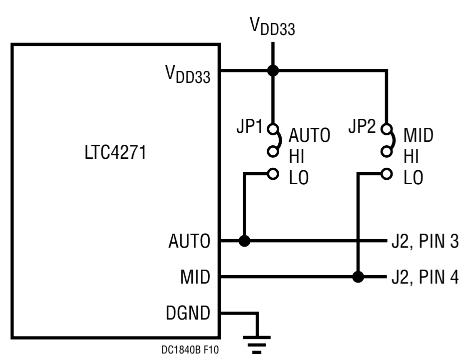


Figure 10. DC1682B AUTO and MID Jumpers

DEMONSTRATION CIRCUIT 1682B OPERATION

AUTO and MID Jumpers

The AUTO and MID pins of the LTC4271 are set by jumpers JP1 and JP2 respectively on the DC1682B (Figure 10). Setting JP1 to HI enables the AUTO pin mode in the LTC4270/LTC4271 chipset. J2 provides test points for access to AUTO and MID.

In AUTO pin mode (JP1 high), the LTC4270/LTC4271 chipset internal I^2C registers default to the AUTO pin high state after a software or hardware reset, or system power on. The LTC4270/71 chipset autonomously detects, powers on and disconnects power to PDs without the need for I^2C host control.

Setting JP1 to LO disables AUTO pin mode and sets the LTC4270/LTC4271 chipset to a low current shutdown mode. An I^2C host controller can then be used to configure the LTC4270/LTC4271 chipset to semi-auto mode for controlled PSE operation or to manual mode for test purposes.

Setting JP2 to HI enables the midspan mode detection backoff timer in the LTC4270/LTC4271 chipset. For endpoint PSEs, set JP2 to LO to disable midspan mode.

For quick PSE evaluation in AUTO pin mode with MIDSPAN disabled, set JP1 HI and JP2 LO on the DC1682B.

Surge Protection

Ethernet ports can be subject to significant cable surge events. To keep PoE voltages below a safe level and protect the application against damage, protection components, as shown in Figure 11, are required at the main supply, at the LTC4270 supply pins and at each port.

Bulk transient voltage suppression (TVS_{BULK}) and bulk capacitance (C_{BULK}) are required across the main PoE supply and should be sized to accommodate system level surge requirements.

Each LTC4270 requires a 10Ω, 0805 resistor (R1) in series from supply AGND to the LTC4270 AGND pin. Across the LTC4270 AGND pin and V_{EE} pin are an SMAJ58A, 58V TVS (D1) and a 1µF, 100V bypass capacitor (C19). These components must be placed close to the LTC4270 pins.

Finally, each port requires a pair of S1B clamp diodes: one from OUTn to supply AGND and one from OUTn to supply V_{EE}. The diodes at the ports steer harmful surges into the supply rails where they are absorbed by the surge suppressors and the V_{EE} bypass capacitance. The layout of these paths must be low impedance. These S1B diodes are placed on the DC1680 mother board of the DC1840 kit.

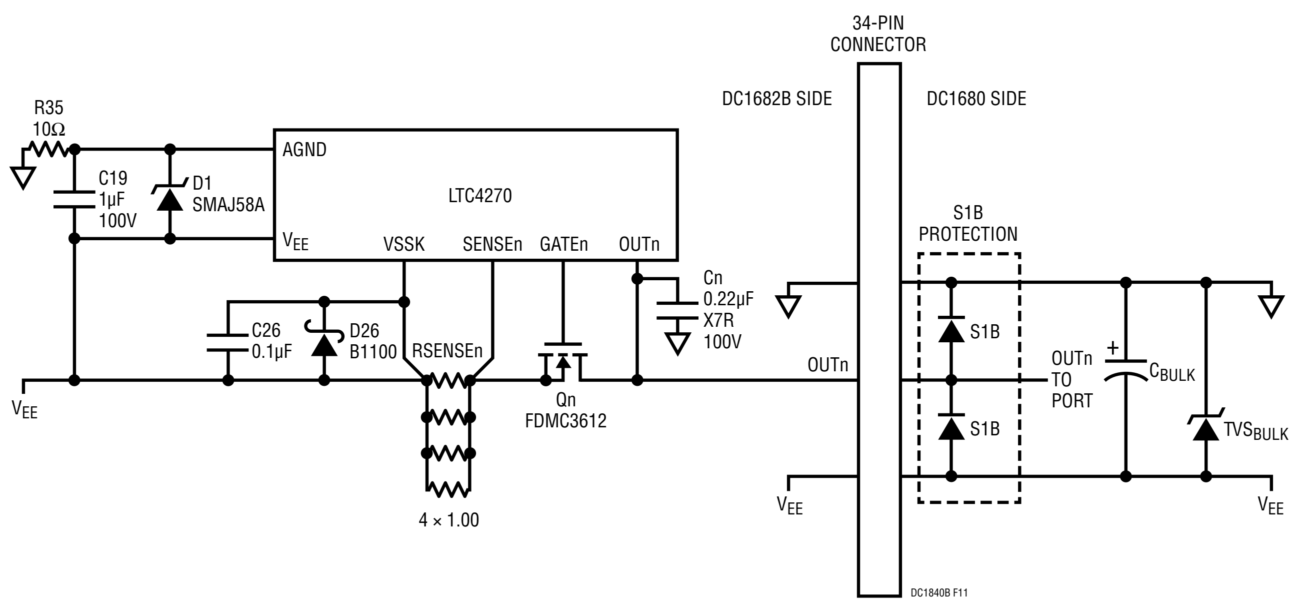


Figure 11. DC1682B, 1 of 12 Ports Surge Protection

DEMONSTRATION CIRCUIT 1680A OPERATION

Demonstration circuit 1680A is a 12-Port, IEEE802.3at Type 1 and Type 2 PoE PSE mother board. This board accepts various PSE daughter cards featuring Linear Technology PSE controllers. The DC1680A is capable of powering up to 12 PDs.

Daughter Card Insertion Precautions

When inserting or removing the daughter card into the DC1680A, verify all supplies and LEDs are off. Push the card straight down for insertion or pull straight up for removal to avoid bending the connector pins. Follow the instructions in the Quick Start Procedure for alignment.

V_{EE} Supply

Connect a power supply for V_{EE} with the positive rail to POS and negative rail to NEG as shown in Figure 3 of the Quick Start Procedure. Set the voltage within the range in Table 1 depending on whether the application is a Type 1 or Type 2. Choose a power supply rating and set the current limit high enough to provide power for the maximum number of PDs connected and to meet each PD power requirements.

Table 1. DC1680A V_{EE} Power Range for Type 1 and Type 2 PSEs

PSE TYPE	V_{EE} SUPPLY RANGE	MAX DELIVERED PORT POWER	POWER SUPPLY*
Type 1	45V to 57V	13W	300W
Type 2	51V to 57V	25.5W	600W

*Recommended DC1840A power supply minimum to avoid dropping in a worst-case scenario with I_{LIM} current at all 12 ports.

PD Connection

PDs are connected using an Ethernet cable to any of the 12 ports at the 2×6, RJ45 connector J4 on the DC1680A (Figure 3). J4 has an integrated Ethernet transformer and common mode termination for each port. Test points for port outputs OUT1 through OUT12 are provided.

DC1680A USER FEATURES

Refer to Figure 12 and Figure 13 for the following user features.

Onboard 3.3V Supply

The DC1680A has an onboard V_{DD33} digital supply generated from the V_{EE} supply. V_{DD33} is tied to AGND, and DGND is a negative voltage referenced to AGND. If an external 3.3V supply is to be used, contact Linear Technology Applications for proper connection.

V_{EE} and V_{DD33} LED Indicators

LEDs for V_{EE} and V_{DD33} indicate if voltage is present at these supplies. Verify these LEDs are off before inserting or removing the daughter card.

Digital Connections

The DC1680A has connections for I^2C control from a host controller. The DC590 is optionally connected to the DC1680A at J5 through a 14-pin ribbon cable. The QuikEval software will automatically detect the DC1680A and open the LTC4271 GUI. Refer to the LTC4271 PSE Demo Software User Manual document for instructions on using the GUI. A second 14-pin ribbon cable can be connected to J6 for I^2C expansion to another DC1680A board with slight board modifications. Contact Linear Technology Applications for instructions.

Digital test points include SCL, SDA, DGND, $\overline{INT}$, $\overline{MSD}$, and $\overline{RESET}$. I^2C address pin AD6, AD3, and AD2 are set with a 3-bit switch SW3.

Midspan PSE

The DC1840A can be configured as a midspan PSE. Upstream switch data comes in to J3. Data and PoE go out to a PD at J4. Set both MID and AUTO pins logic high.

DEMONSTRATION CIRCUIT 1680A OPERATION

$\overline{\text{MSD}}$ and $\overline{\text{RESET}}$ Pushbuttons

Pushbutton switch SW1, when pressed, pulls the $\overline{\text{RESET}}$ pin of the daughter card logic low. The PSE controller is then held inactive with all ports off and all internal registers reset to their power-up states. When SW1 is released, $\overline{\text{RESET}}$ is pulled high, and the PSE begins normal operation.

Pushbutton switch SW2 when pressed pulls the maskable shutdown input ($\overline{\text{MSD}}$) pin of the daughter card logic low. When pressed, all ports that have their corresponding mask bit set in the mconfig register of the PSE controller will be shutdown. These ports must then be manually re-enabled via I^2C or by resetting the PSE.

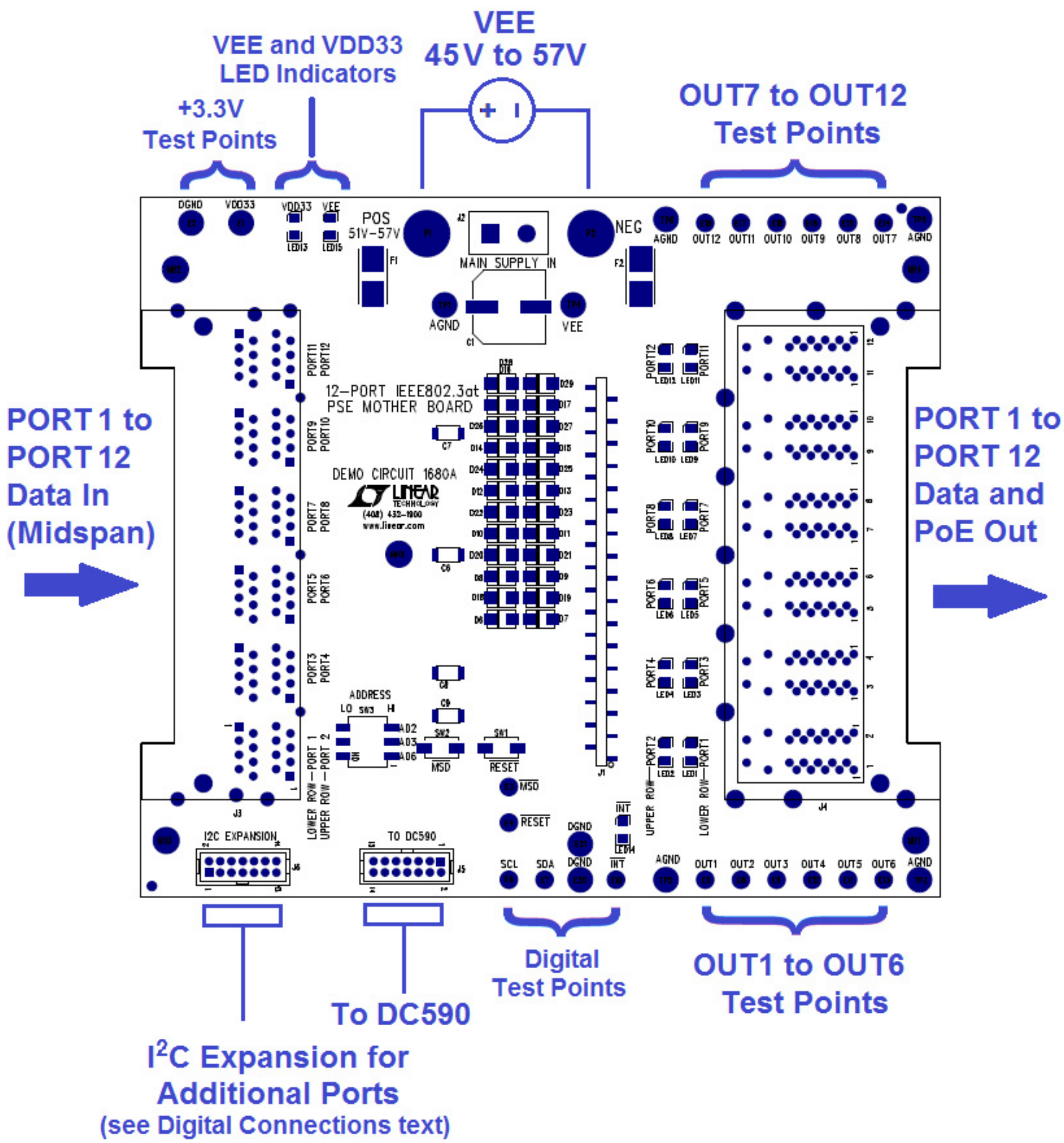


Figure 12. DC1680A Connections and Supply LEDs

DEMONSTRATION CIRCUIT 1680A OPERATION

Interrupt LED

A red LED indicates when the $\overline{INT}$ line is pulled logic low by the daughter card. When the interrupt is cleared (high) via I^{2}C servicing, the LED is turned off.

Port 1 Through 12 Power LED Indicators

Each PSE port has a green LED indicator to show when PoE power is present at the port. The LEDs are driven by the respective port OUT voltage.

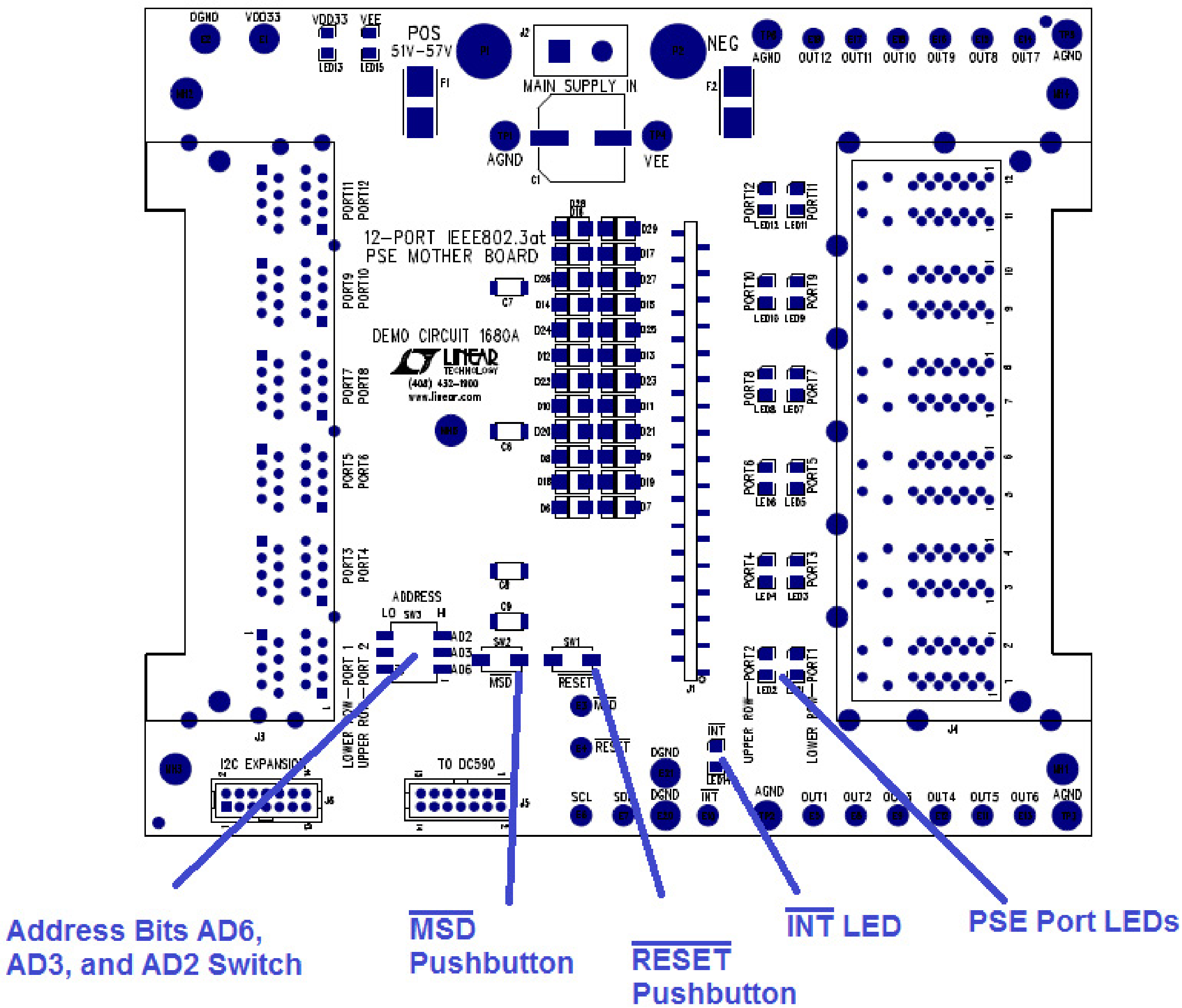


Figure 13. DC1680A Address Switch, Pushbutton Switches, INT LED, and Port Power LEDs

DEMONSTRATION CIRCUIT 1840 SYSTEM

DC1840 System Setup

Figure 14 shows a basic DC1680A system setup. The DC1682 daughter card is inserted in the 34-pin connector J1. A power supply is connected to V_{EE} with banana cables. The DC590 connects with 14-pin ribbon cable to the DC1680A and to a PC via USB. On the PC a GUI communicates with the board. At the PSE output, PDs are connected. A sample PD demo board is shown in Figure 14.

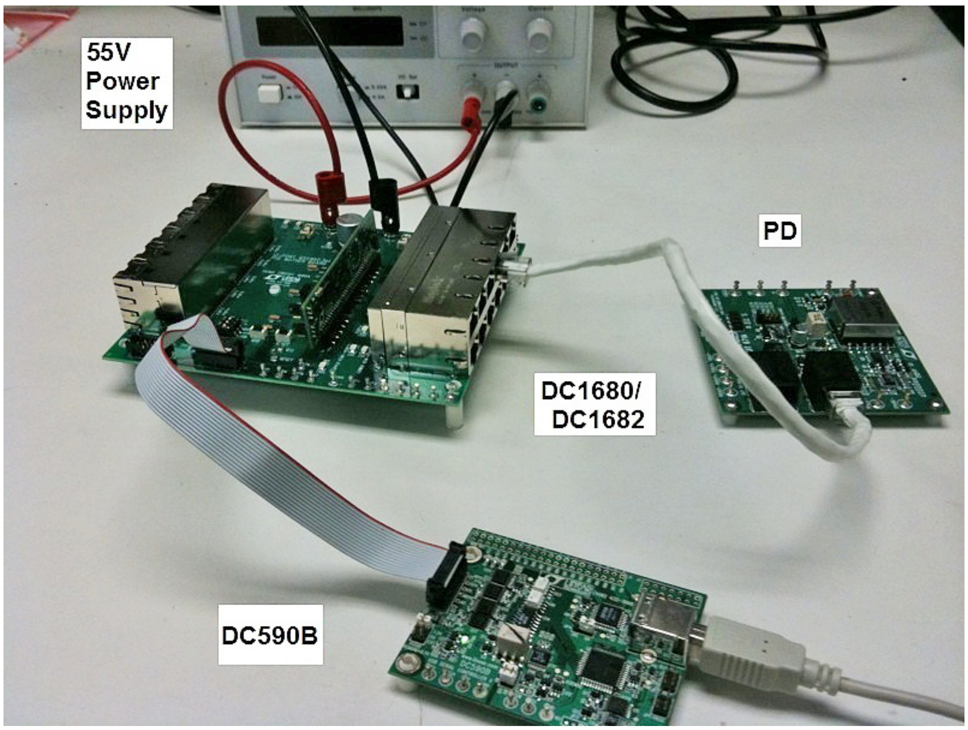


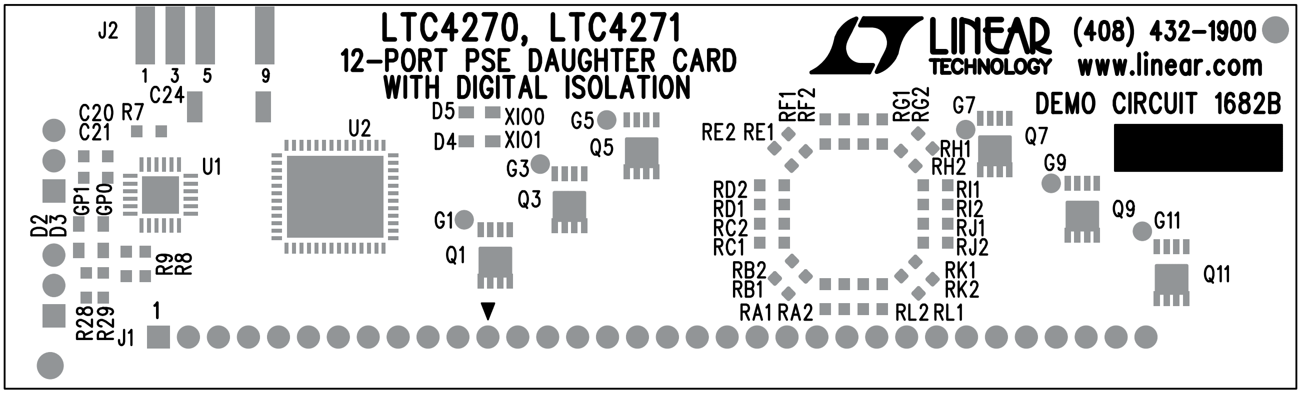
Figure 14. DC1680 and DC1682 System Setup with Power Supply, DC590 and PD Demo Board

Table 2. DC1840 Kit Versions

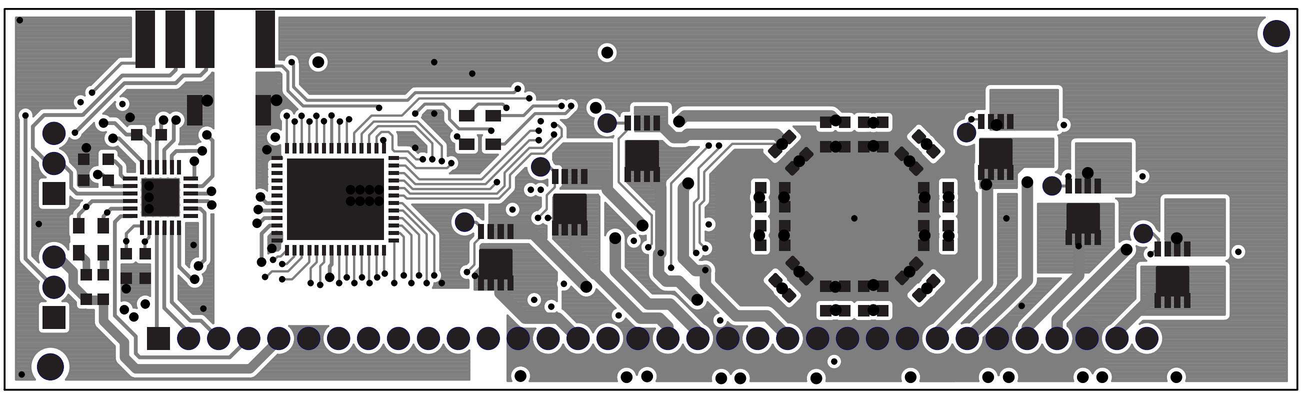
VERSION	FEATURES
DC1840A	DC1680A, Mother Board with Integrated Magjack DC1682A, 12-Port PSE Daughter Card
DC1840B	DC1680A, Mother Board with Integrated Magjack DC1682B, 12-Port PSE Daughter Card with Increased Surge Protection

DEMONSTRATION CIRCUIT 1682A LAYOUT

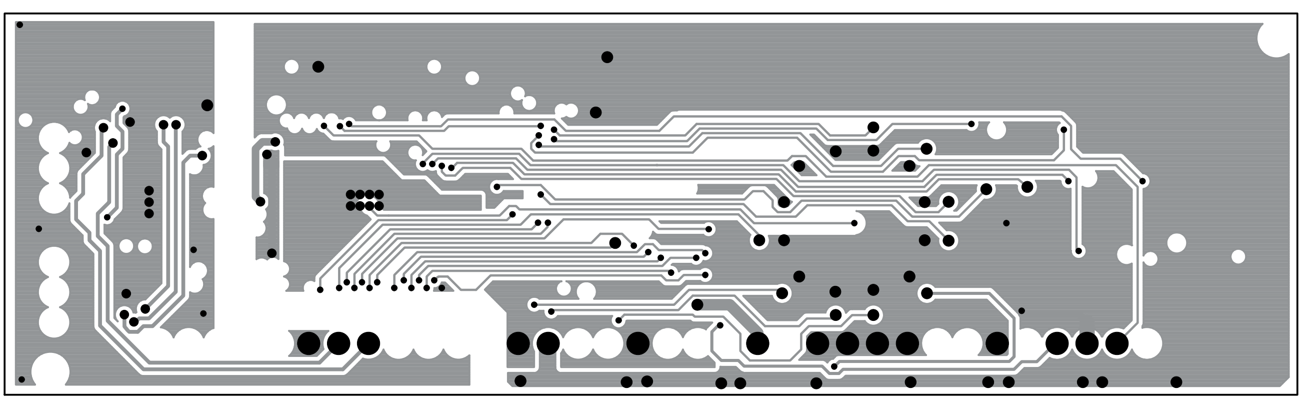
Top Assembly



Layer 1: Top Layer

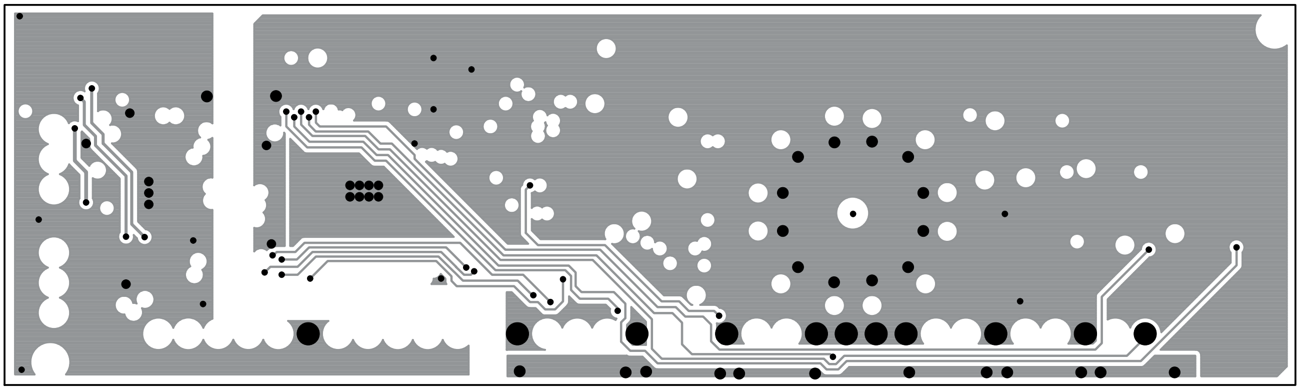


Layer 2: V_{EE} Plane 1

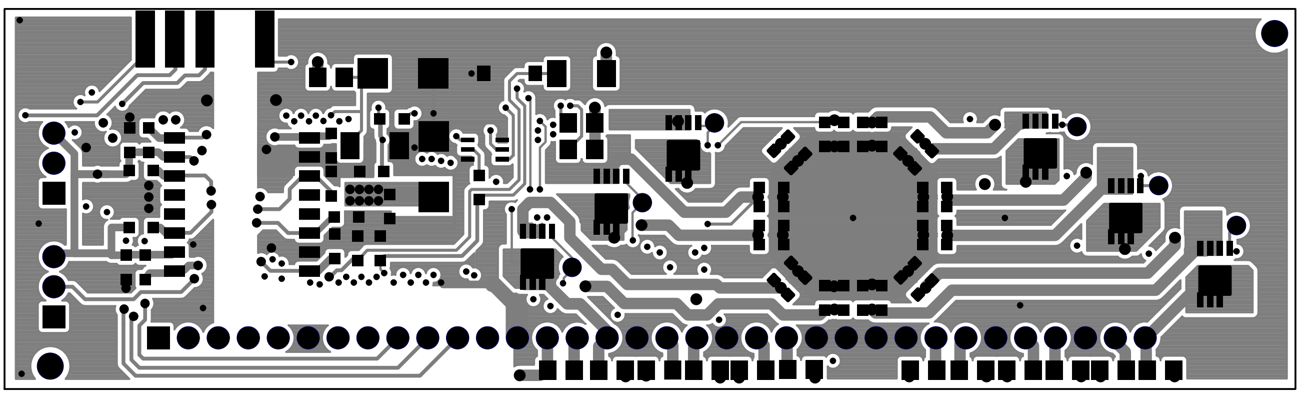


DEMONSTRATION CIRCUIT 1682A LAYOUT

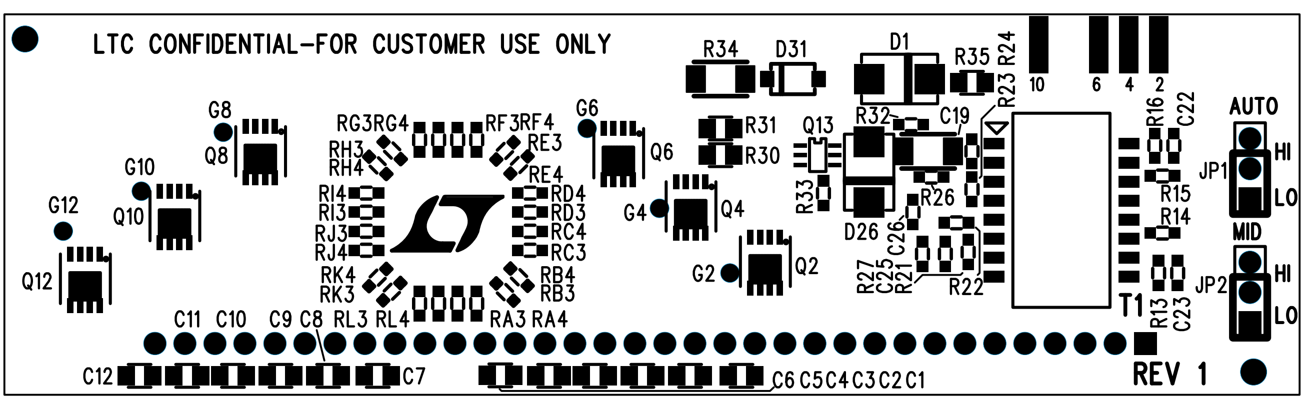
Layer 3: V_{EE} Plane 2



Layer 4: Bottom Layer

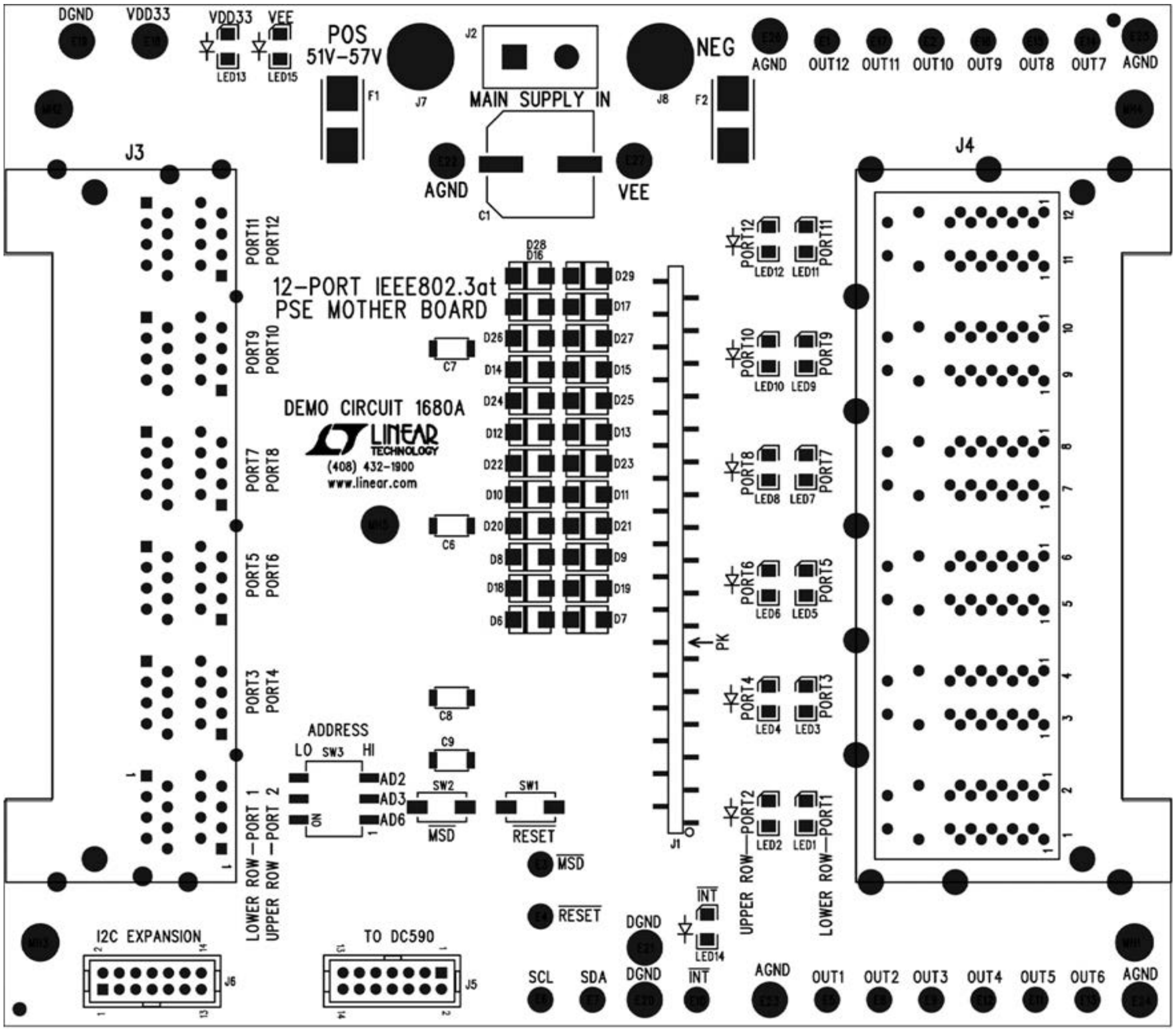


Bottom Assembly



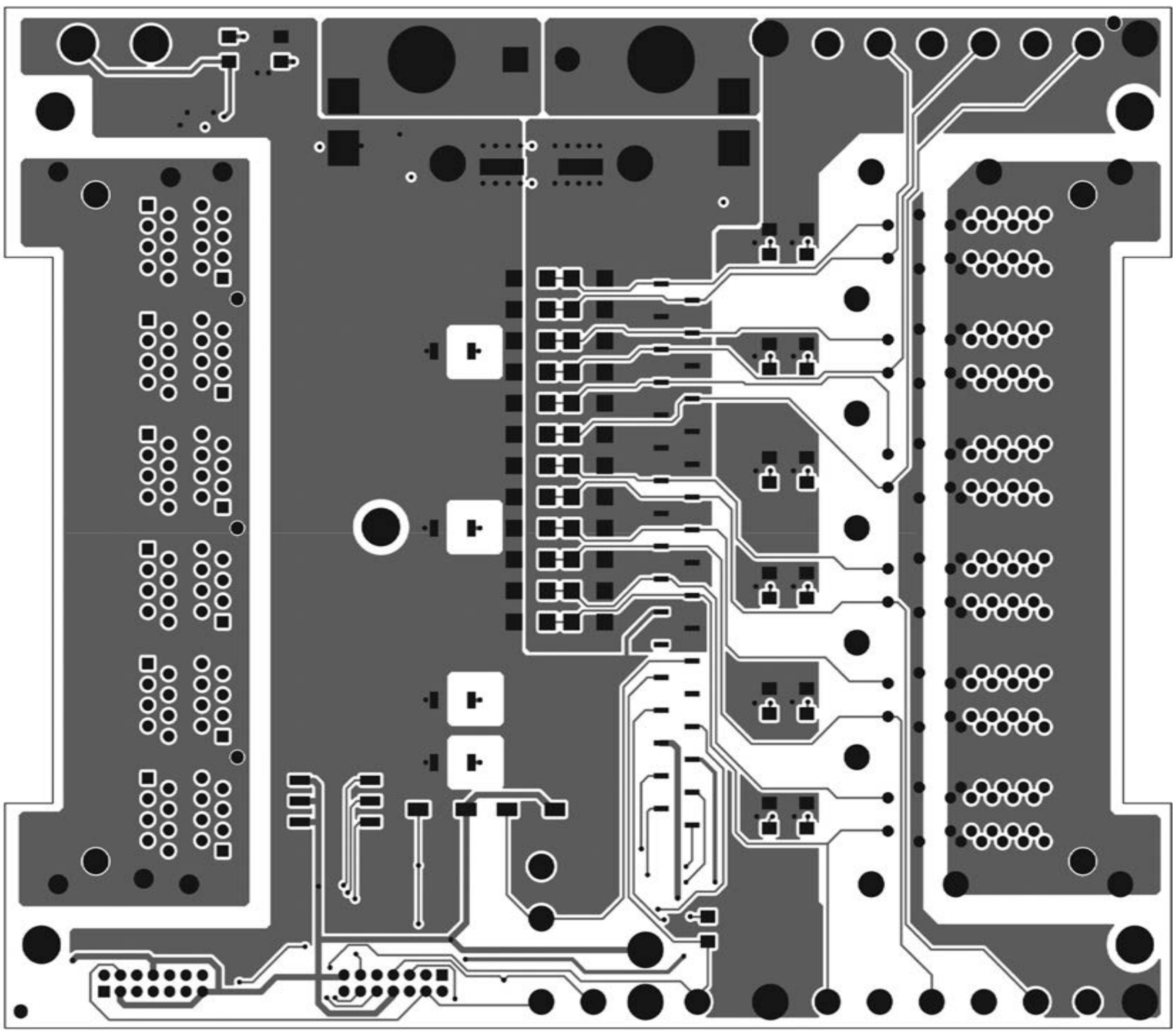
DEMONSTRATION CIRCUIT 1680A LAYOUT

Top Silkscreen



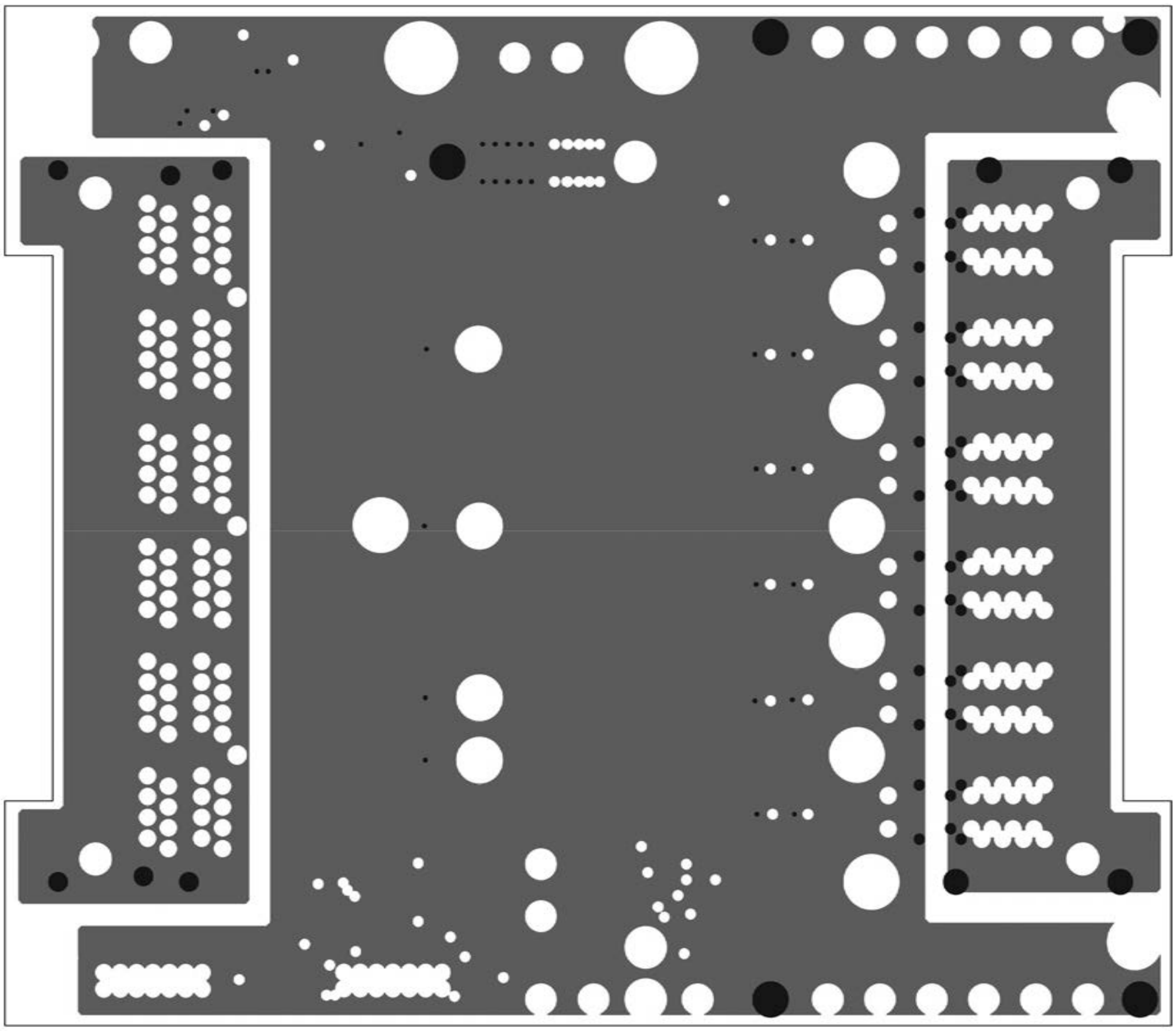
DEMONSTRATION CIRCUIT 1680A LAYOUT

Layer 1: Top Layer



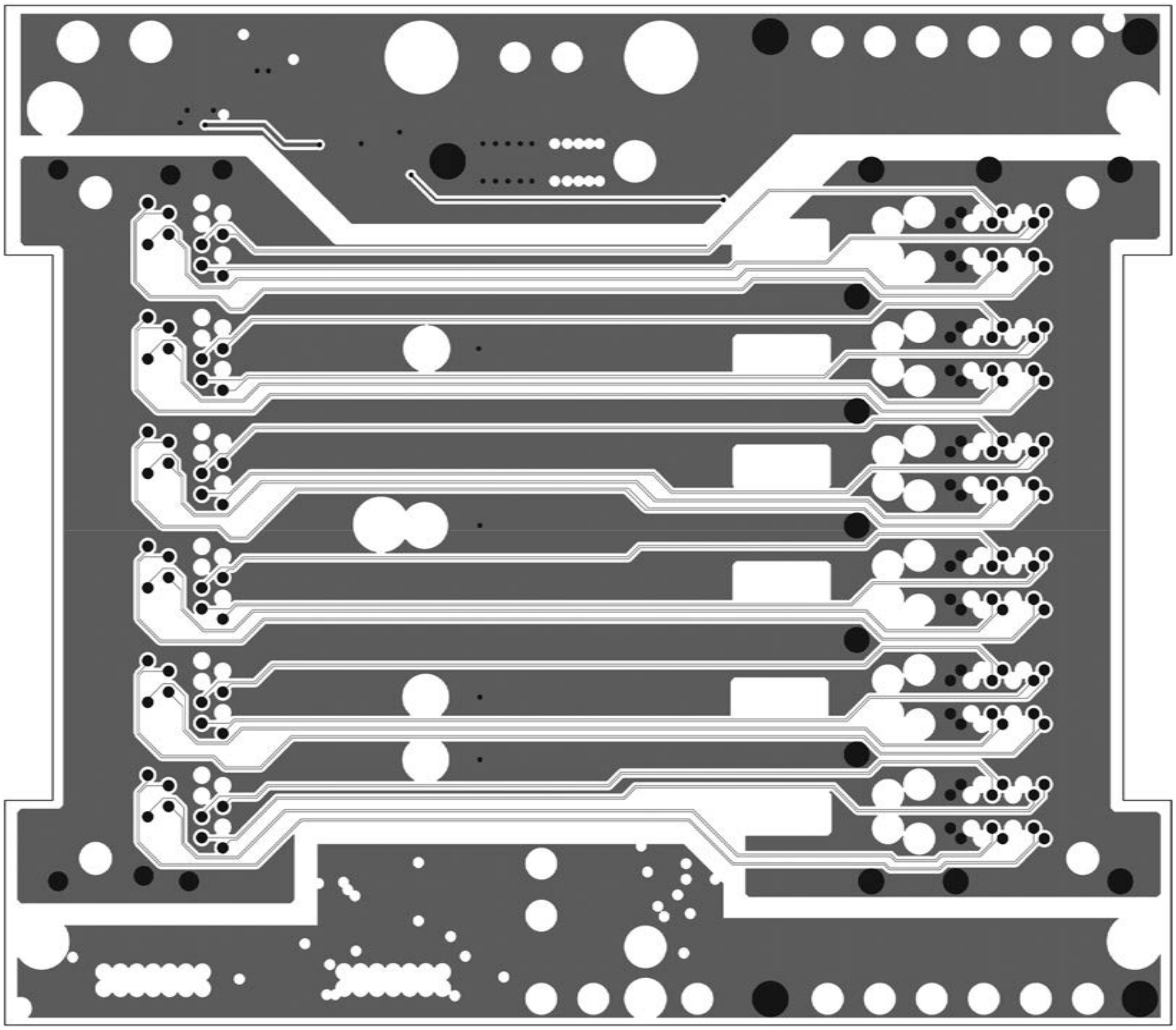
DEMONSTRATION CIRCUIT 1680A LAYOUT

Layer 2: AGND, CGND Plane 1



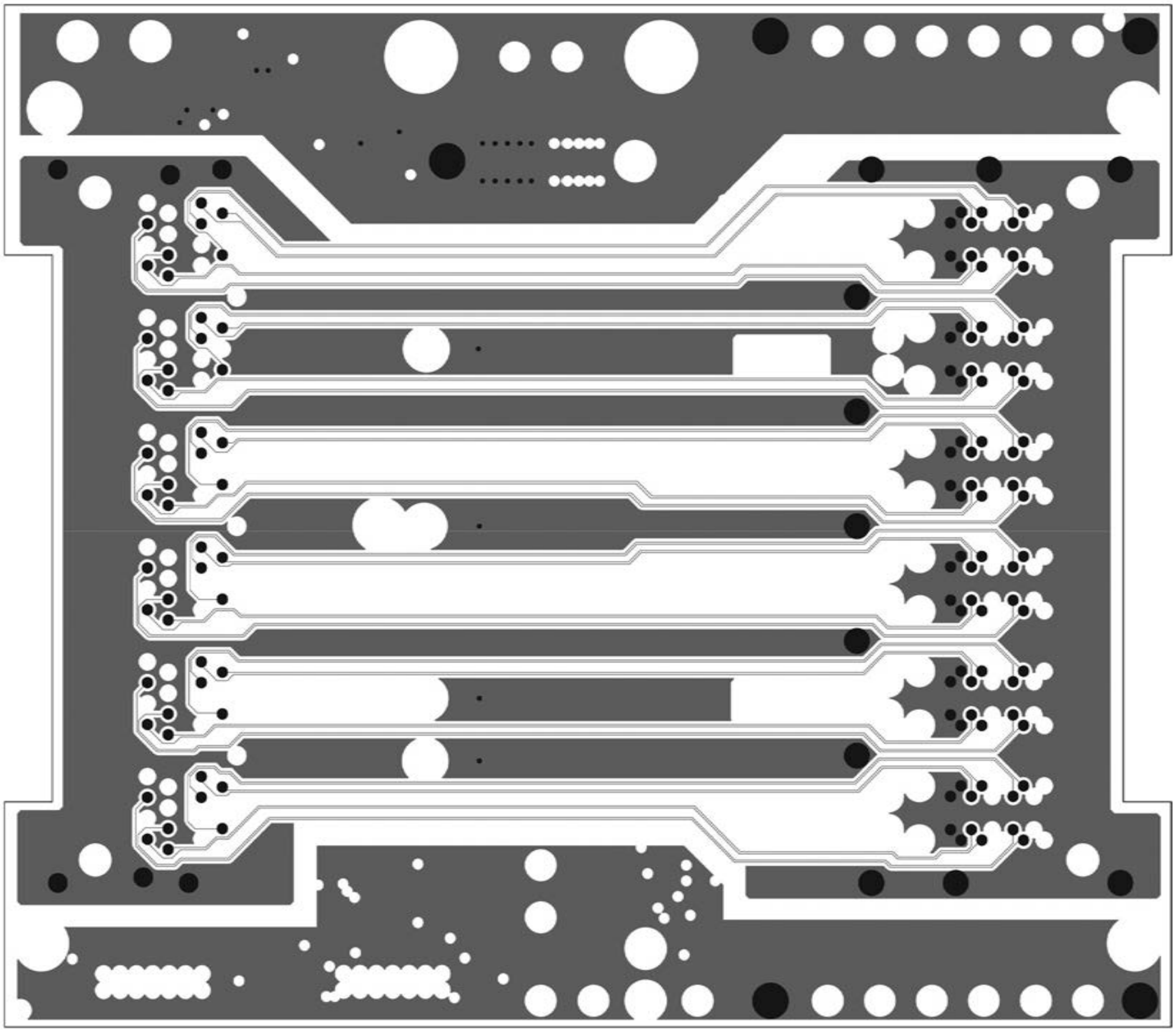
DEMONSTRATION CIRCUIT 1680A LAYOUT

Layer 3: SIG, AGND, CGND Plane 2



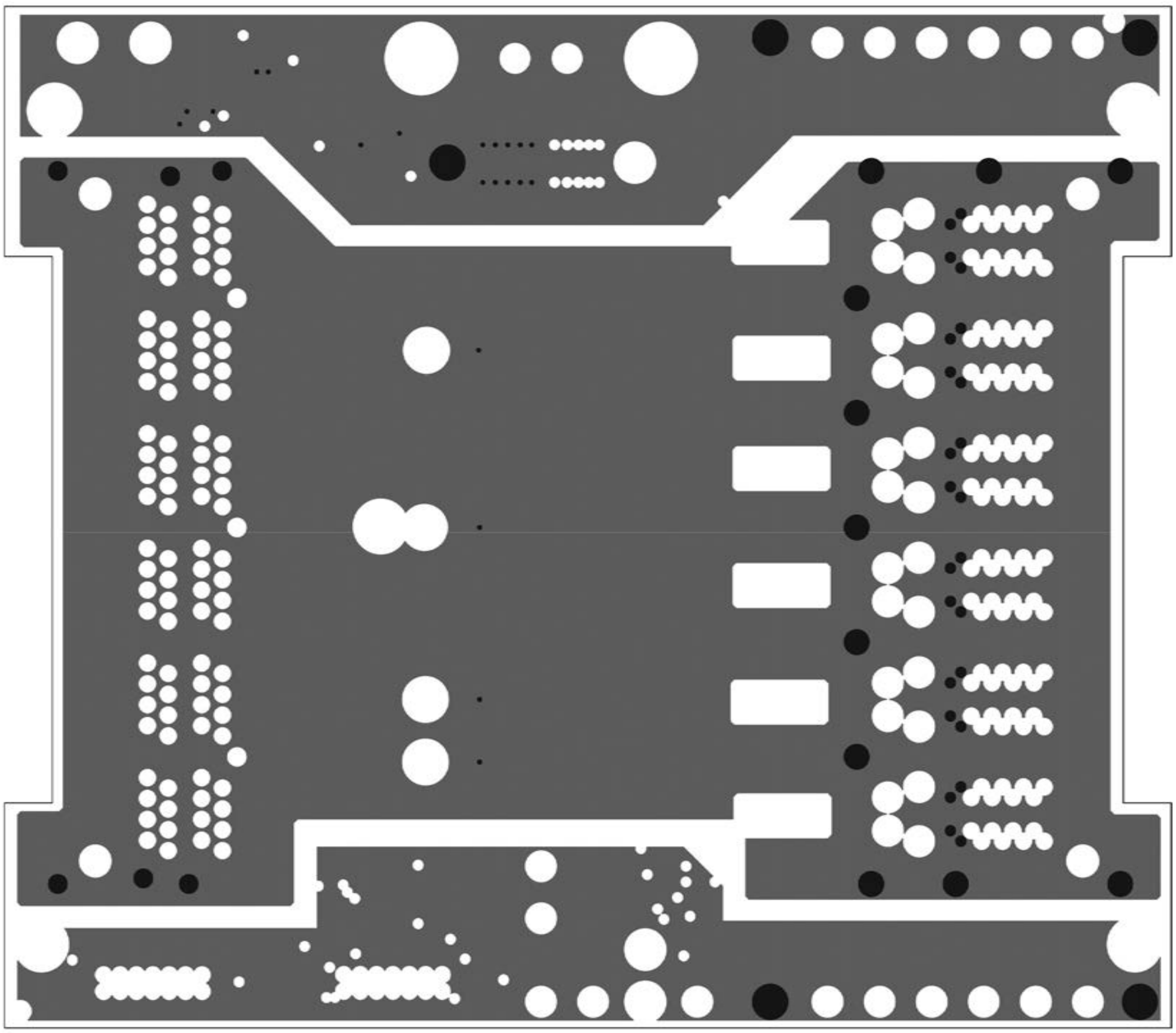
DEMONSTRATION CIRCUIT 1680A LAYOUT

Layer 4: SIG, AGND, CGND Plane 3



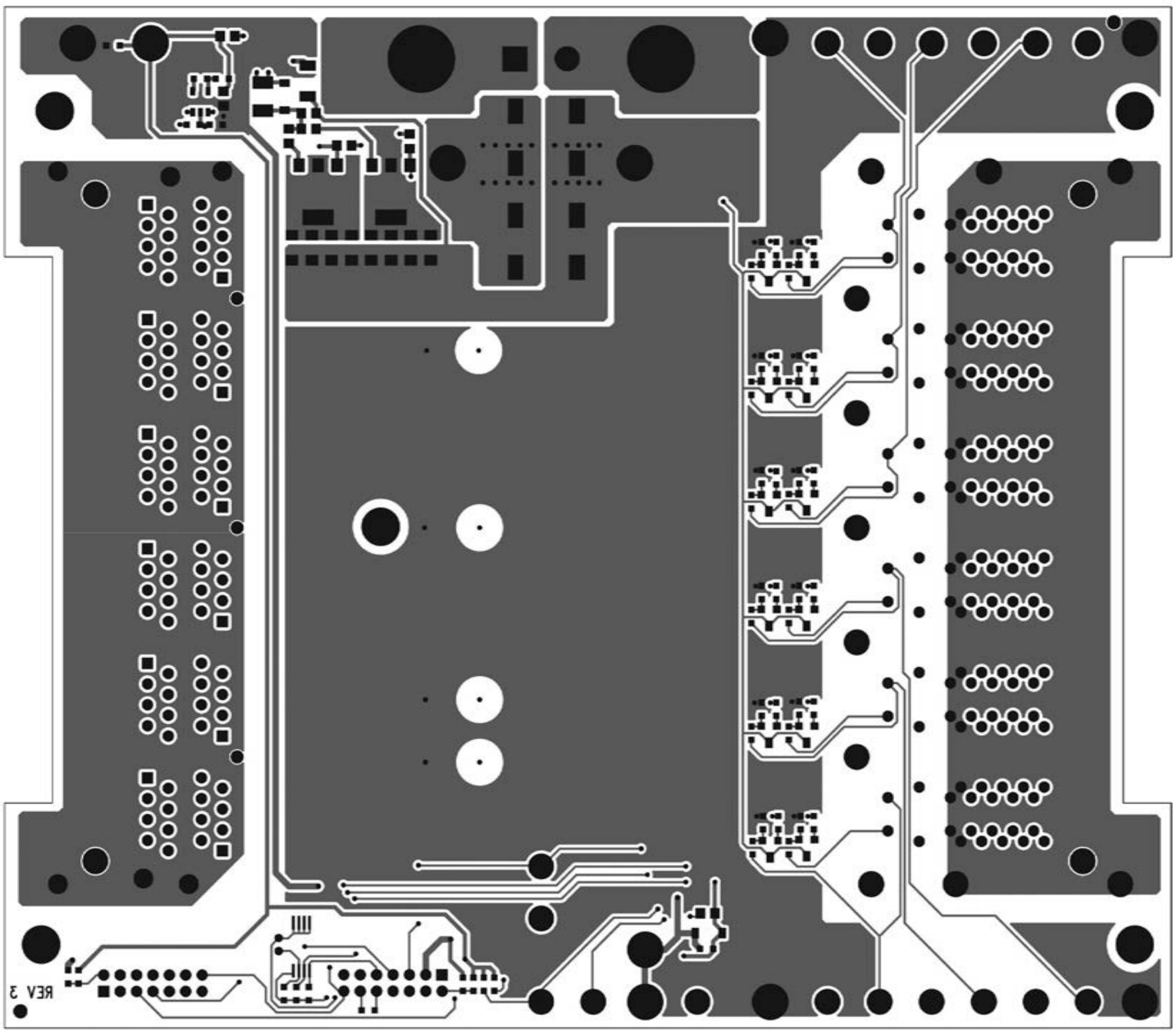
DEMONSTRATION CIRCUIT 1680A LAYOUT

Layer 5: SIG, CGND, CGND Plane 4



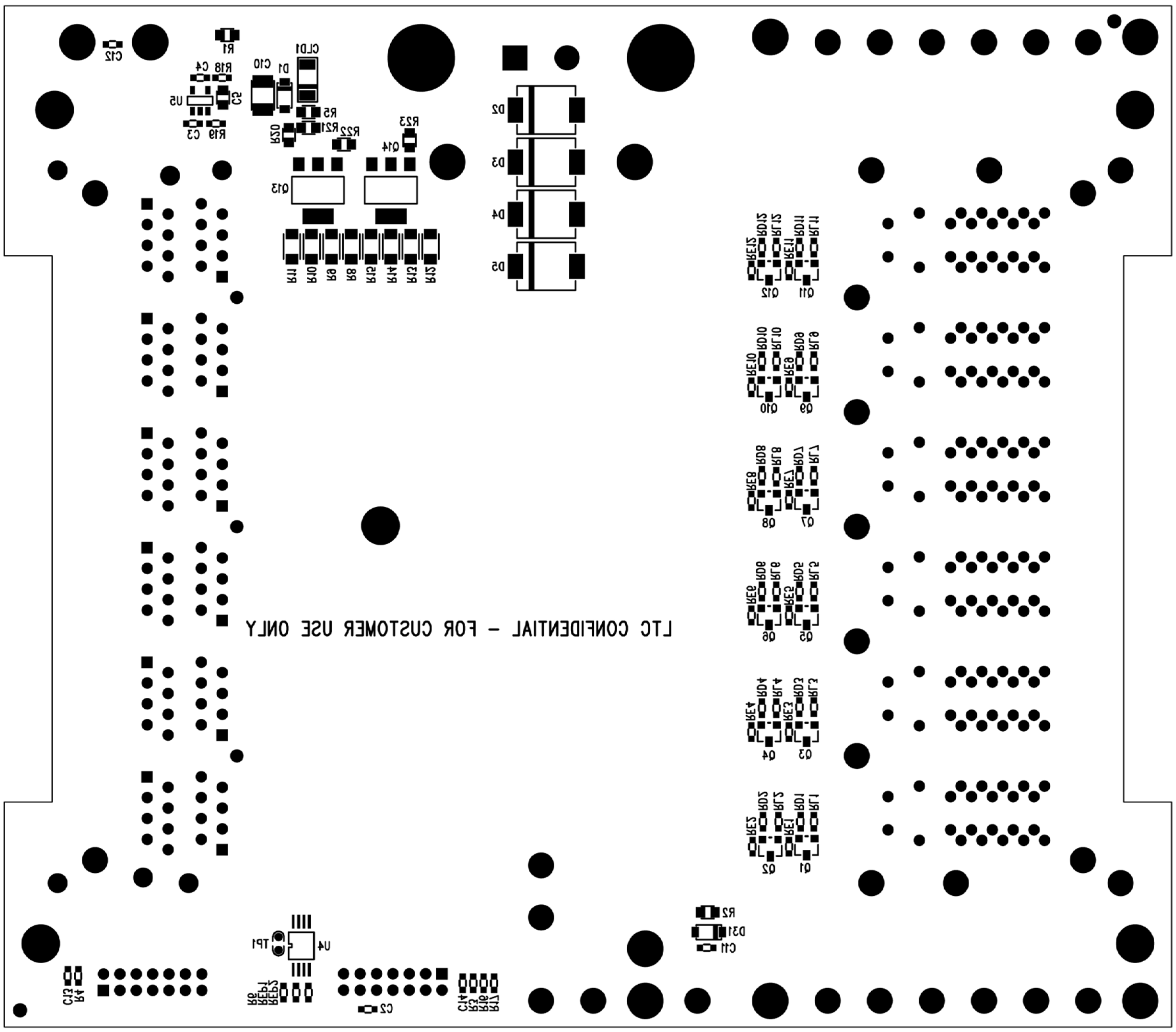
DEMONSTRATION CIRCUIT 1680A LAYOUT

Layer 6: Bottom Layer

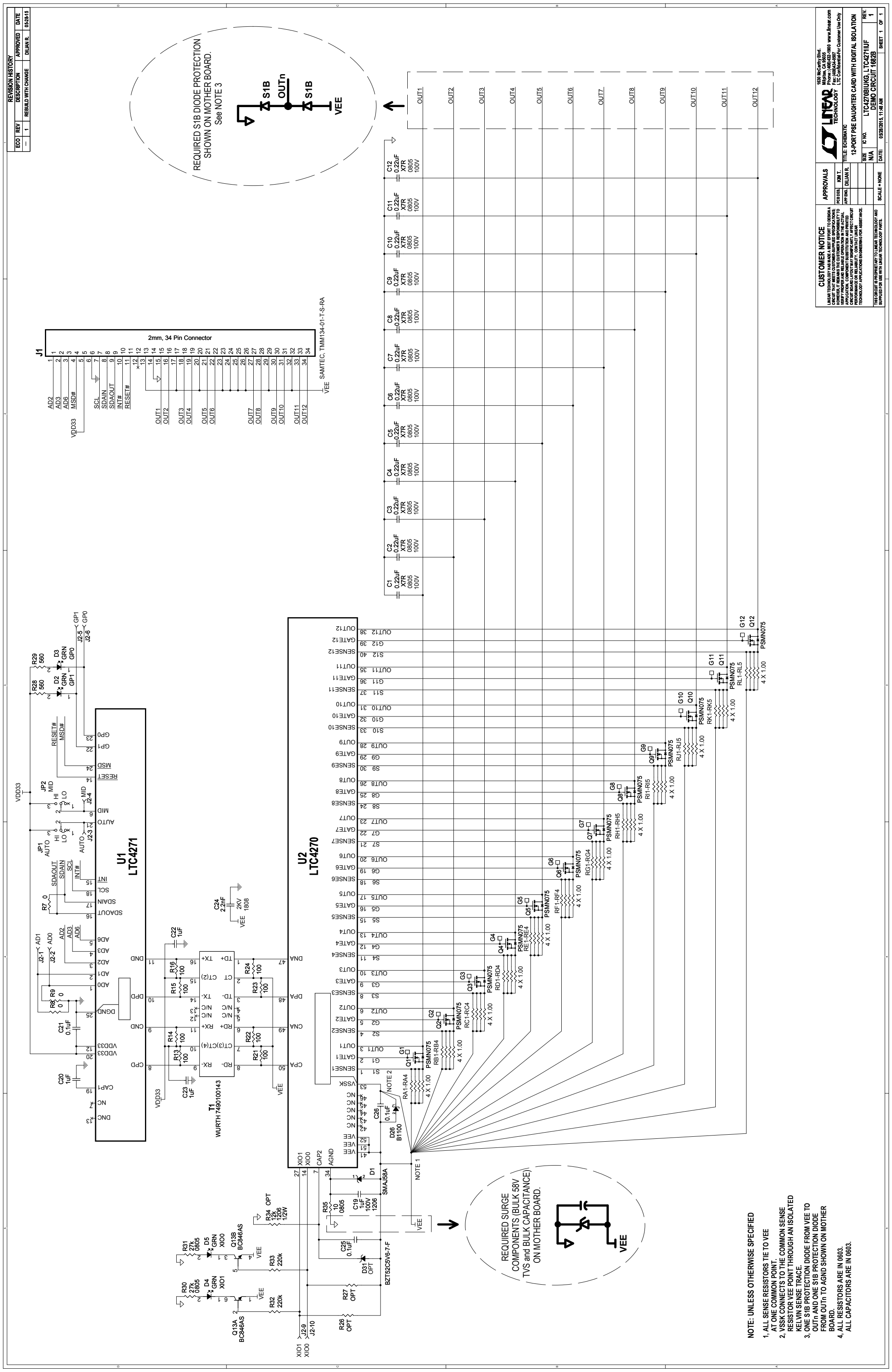


DEMONSTRATION CIRCUIT 1680A LAYOUT

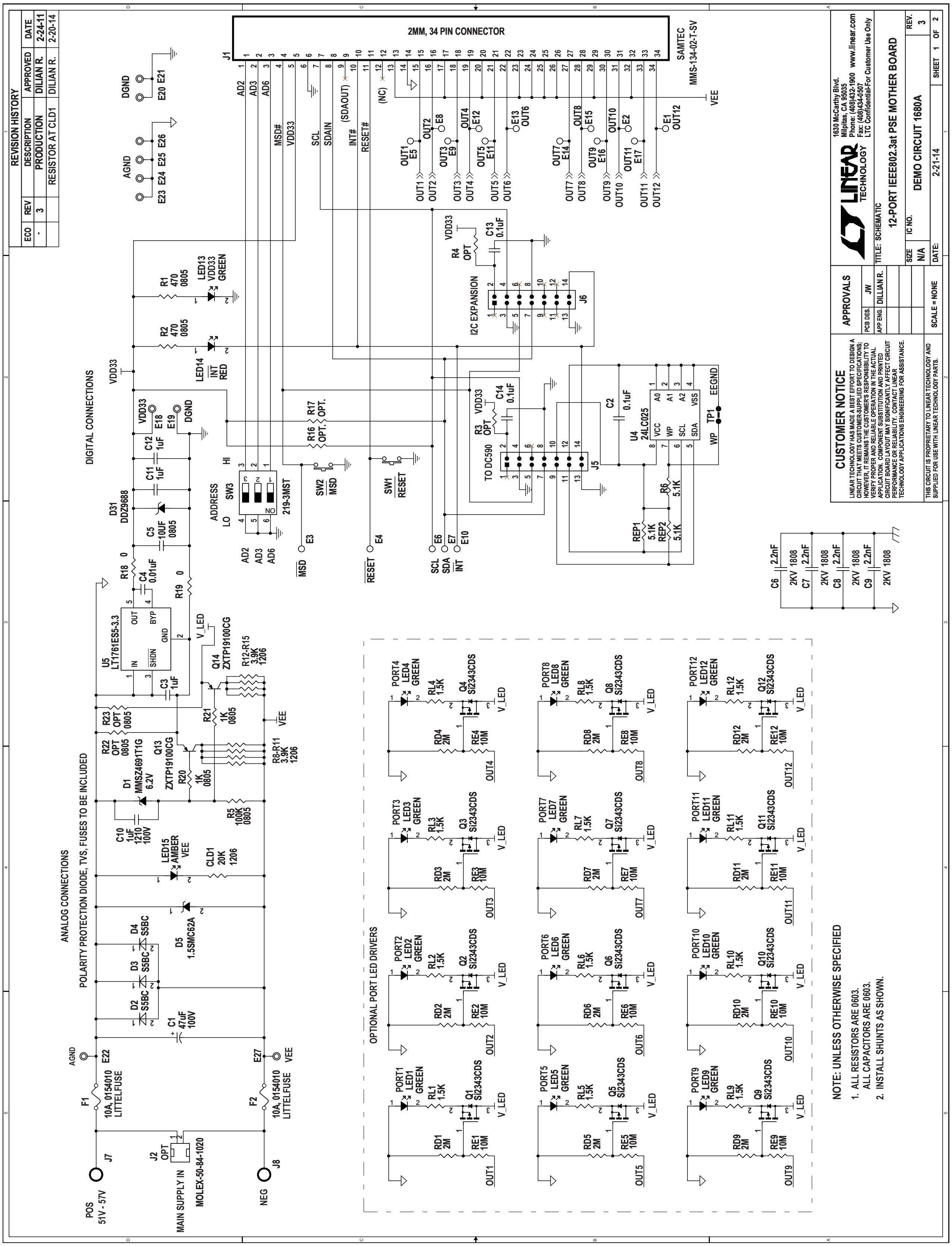
Bottom Silkscreen



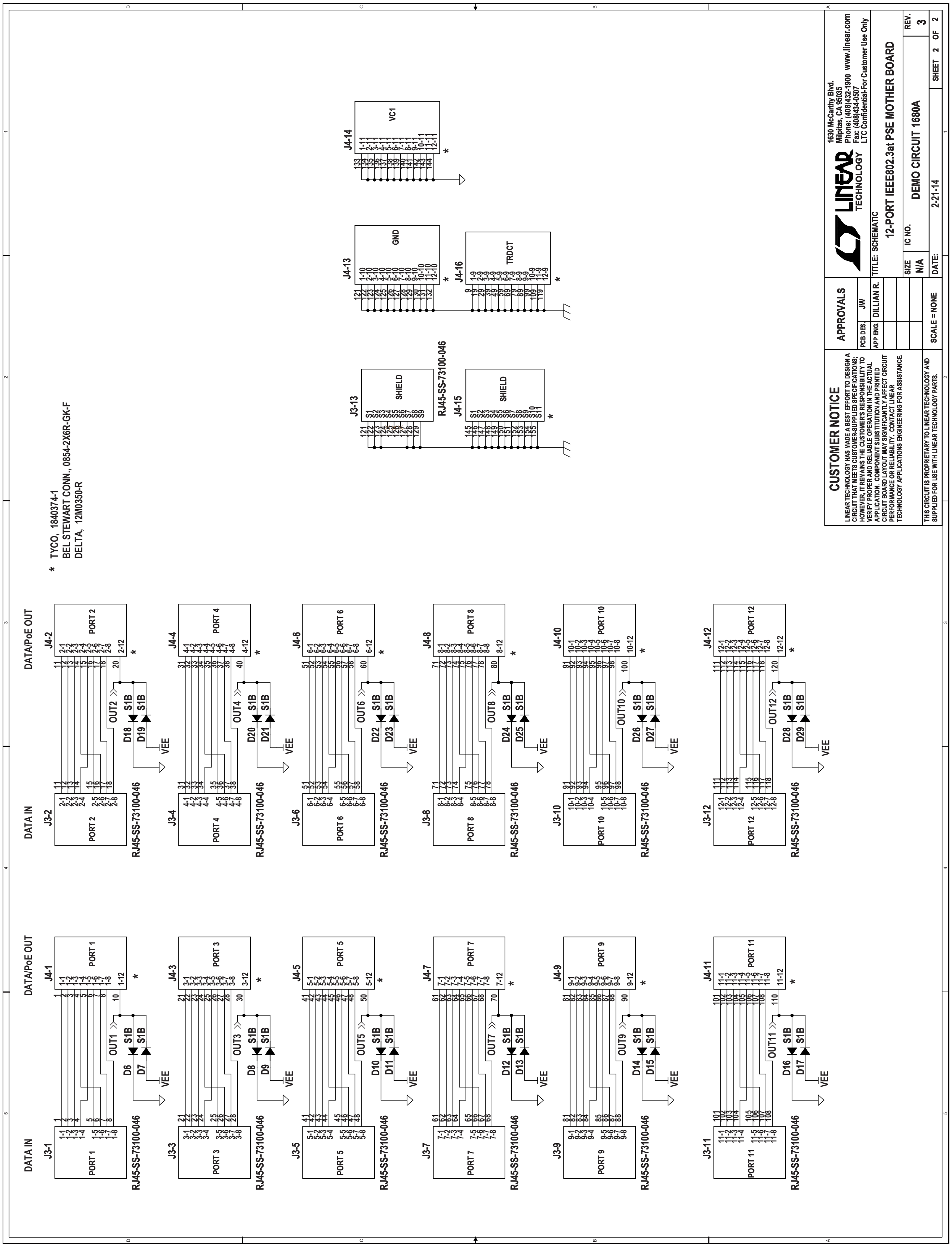
DC1682A SCHEMATIC DIAGRAM



DC1680A SCHEMATIC DIAGRAM



DC1680A SCHEMATIC DIAGRAM



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If this evaluation kit does not meet the specifications recited in the DEMO BOARD manual the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY THE SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THIS INDEMNITY, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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